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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,753	09/13/2000	Chin-Huang Chang	6319-56134	7237

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Klarquist Sparkman Campbell
Leigh & Whinston LLP
One World Trade Center Suite 1600
121 S W Salmon Street
Portland, OR 97204

EXAMINER
VINH, LAN

ART UNIT	PAPER NUMBER
1765	13

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/660,753	CHANG, CHIN-HUANG	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/24/2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-40* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. For the purpose of examination, the term "semiconductor unit" is defined as a "flip chip " in page 4 of the specification, the term "the thickness of the semiconductor unit meets an expected specification" is defined as the semiconductor unit reaches a specified thickness ranging from 2 mil to 6 mil in pages 3 and 4 of the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 21, 24-26, 28-31, 34-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyono (US 5,532,189) in view of Hudak et al (US 5,656,552)

Kiyono discloses a method for making a semiconductor package. The package including a carrier 2 and a semiconductor unit, the semiconductor unit includes a first surface 10 and a second surface 7, the surface 7 having no electrical connection (fig. 2) This method comprises the steps of:

attaching the first surface 10 to the carrier 2 (fig. 1), the semiconductor package having an LOC (Lead -on-chip) structure (col 2, lines 57-60), which reads on attaching at least a part of the first surface to the carrier according to a configuration of lead-on-chip packaging

etching the surface 7/second surface to reduce the thickness of surface region (col 4, lines 16-22) which reads on etching the semiconductor unit from the second surface to reduce the thickness

Unlike the instant claimed invention as per claims 21, 31, Kiyono does not specifically discloses etching the semiconductor unit from the second surface to reduce semiconductor unit volume until the size of the semiconductor unit meets an expected specification/ the semiconductor unit reaches a thickness ranging from 2 mil to 6 mil

However, Hudak discloses a method for making thin conformal IC (integrated circuit) chip module comprises the step of etching the bottom surface of the die to thin down/ reduce the thickness of the IC die to 50 microns or approximately 2 mils (25.4 microns equal 1 mil) (see prior art of record for evidence of this basis) (col 8, lines 20-22). Husak's etching step reads on etching the surface of the IC die/semiconductor unit until the size of the semiconductor unit meets an expected specification/ the semiconductor unit reaches a specified thickness ranging from 2 mil to 6 mil

Since both Kiyono and Hudak are concerned with method of etching to reduce the thickness of a IC die, one skilled in the art would have found it obvious to modify Kiyono's etching step by etching the surface of the IC die/semiconductor unit until the size of the semiconductor unit meets an expected specification as per Hudak since Hudak teaches that by thinning the IC die to a thickness less than or equal to 50 microns / 2mil, a planarization step required by prior art method may be eliminated (col 4, lines 65-67)

The limitation that the expected specification means that the thickness of the semiconductor unit measured relative to the first surface is within a specified range, as recited in claims 24, 34, has been discussed above

Regarding claim 25, Kiyono discloses using bonding wire in the package (col 4, lines 4-5)

Regarding claims 26, 28, 37, fig. 2 shows that the semiconductor unit is shielded by the fillet 11/fixture during etching.

Regarding claims 29, 36 Kiyono discloses using phenol type adhesive in the semiconductor package (col 4, lines 30-31)

Regarding claims 30, 35, Kiyono discloses that the semiconductor unit includes the bonding wire/electrical connection device to the carrier 2 (fig. 2)

4. Claims 22-23, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyono (US 5,532,189) in view of Hudak et al (US 5,656,552) and further in view of Goruganthu et al (US 6,069,366)

Kiyono as modified by Hudak has been discussed above in paragraph 3. Unlike the instant claimed invention as per claims 22-23, 32, Kiyono and Hudak do not disclose etching the semiconductor unit by using beams of light or plasma.

However, Goruganthu discloses a method for thinning of a chip bonded integrated circuit comprises the step of using beam of light/ RIE (plasma etching) to etch the semiconductor unit (col 5, lines 56-57; col 6, lines 11-12)

Since Kiyono is concerned with a method of reducing the thickness of one surface the semiconductor unit, one skilled in the art would have found it obvious to modify Kiyono and Hudak by etching the semiconductor unit by using beams of light or plasma as per Goruganthu because Goruganthu teaches that the laser process is suitable for both local and global thinning over a part or the whole surface of the backside of the die/semiconductor unit (col 5, lines 64-67)

5. Claim 27, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyono (US 5,532,189) in view of Hudak et al (US 5,656,552) and further in view of Siniaguine (US 6,184,060)

Kiyono as modified by Hudak has been described above in paragraph 3. Unlike the instant claimed inventions as per claim 7, Goruganthu and Hudak do not specifically disclose the step of grinding the IC die/semiconductor unit to a expected specification/ a specified thickness range before joining the IC die to the carrier although Goruganthu does disclose using a grinding device to thin the die (col 5, lines 40-42).

However, Siniaguine discloses a method for fabricating semiconductor die comprises the step of grinding the semiconductor wafer/unit to reduce the thickness of the semiconductor wafer/unit to a specified thickness before dicing the wafer into chip (col 8, lines 48-50)

Hence, one skilled in the art would have found it obvious to modify Goruganthu and Hudak grinding step by grinding the die/semiconductor unit to reduce the thickness to a specified thickness as taught by Siniaguine since Siniaguine states that it is known that

silicon is removed from the semiconductor wafer/semiconductor unit by mechanical grinding to reduce the wafer thickness to a specified range (col 8, lines 47-50)

6. Claims 39, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyono (US 5,532,189) in view of Hudak et al (US 5,656,552)

Kiyono discloses a method for making a semiconductor package. The package including a carrier 2 and a semiconductor unit, the semiconductor unit includes a first surface 10 and a second surface 7, the surface 7 having no electrical connection (fig. 2) This method comprises the steps of:

attaching the first surface 10 to the carrier 2 (fig. 1)

using a fillet 11/fixture to cover/surround the carrier and semiconductor unit while exposing the surface 7/second surface (col 4, lines 8-10 ; fig. 2)

etching the surface 7/second surface to reduce the thickness of surface region (col 4, lines 16-22) which reads on etching the semiconductor unit from the second surface to reduce the thickness

Unlike the instant claimed invention as per claim 39, Kiyono does not specifically discloses etching the semiconductor unit from the second surface to reduce semiconductor unit volume until the size of the semiconductor unit meets an expected specification/ the semiconductor unit reaches a thickness ranging from 2 mil to 6 mil

However, Hudak discloses a method for making thin conformal IC (integrated circuit) chip module comprises the step of etching the bottom surface of the die to thin down/ reduce the thickness of the IC die to 50 microns or approximately 2 mils (25.4 microns

equal 1 mil) (see prior art of record for evidence of this basis) (col 8, lines 20-22). Husak's etching step reads on etching the surface of the IC die/semiconductor unit until the size of the semiconductor unit meets an expected specification/ the semiconductor unit reaches a specified thickness ranging from 2 mil to 6 mil

Since both Kiyono and Hudak are concerned with method of etching to reduce the thickness of a IC die, one skilled in the art would have found it obvious to modify Kiyono's etching step by etching the surface of the IC die/semiconductor unit until the size of the semiconductor unit meets an expected specification as per Hudak since Hudak teaches that by thinning the IC die to a thickness less than or equal to 50 microns / 2mil, a planarization step required by prior art method may be eliminated (col 4, lines 65-67)

Regarding claim 40, fig. 1 shows that the fillet 11 covers the carrier and the semiconductor unit except the surface 7/second surface.

Response to Arguments

7. Applicant's arguments with respect to claims 21-40 have been considered but are moot in view of the new ground(s) of rejection.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Myer et al (US 4,872,945) discloses that 25.4 microns being equal to 1mil (col 5, lines 20-22)

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

LV
May 28, 2003